(12) **United States Patent**

Hung et al.

(10) **Patent No.:** **US 9,159,412 B1**

(45) **Date of Patent:** **Oct. 13, 2015**

(54) **STAGGERED WRITE AND VERIFY FOR PHASE CHANGE MEMORY**

(71) Applicant: **Macronix International Co., Ltd.,** Hsinchu (TW)

(72) Inventors: **Chun-Hsiung Hung**, Hsinchu (TW); **Tien-Yen Wang**, Zhubei (TW)

(73) Assignee: **Macronix International Co., Ltd.,** Hsinchu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/331,487**

(22) Filed: **Jul. 15, 2014**

(51) **Int. Cl.**
    G11C 11/34 (2006.01)
    G11C 13/00 (2006.01)

(52) **U.S. Cl.**
    CPC *G11C 13/0064* (2013.01); *G11C 13/0004* (2013.01); *G11C 13/0069* (2013.01); *G11C 2013/0066* (2013.01)

(58) **Field of Classification Search**
    CPC G11C 16/3454; G11C 16/3459; G11C 11/5628
    USPC 365/185.22, 148, 163, 158
    See application file for complete search history.

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Primary Examiner — Son Dinh

(74) *Attorney, Agent, or Firm* — Yiding Wu; Haynes Beffel & Wolfeld LLP

(57) **ABSTRACT**

A method for storing a data value in a memory cell is provided. The data value includes one of a first data value and a second data value respectively represented by a first and a second programmable resistance ranges. The method includes, within a write cycle, storing the first data value in the memory cell by applying a first verify operation having a first verify period and a first write operation having a first write period, or storing the second data value in the memory cell by applying a second verify operation having a second verify period longer than the first verify period and a second write operation having a second write period shorter than the first write period. The write cycle is shorter than a sum of the first write period and the second verify period.

16 Claims, 8 Drawing Sheets
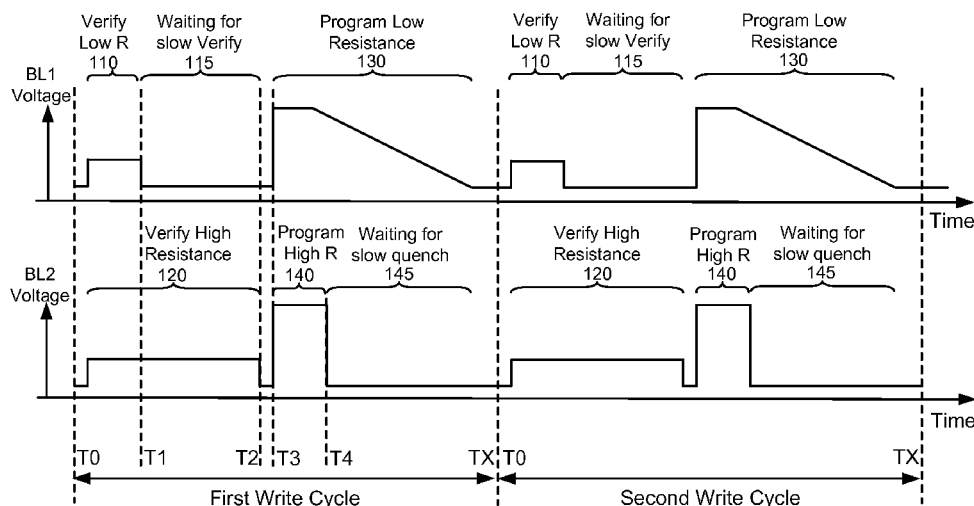
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Figure 1

Figure 2

Figure 3

Figure 4

Figure 5

V3 > V2 > V1

600

Start a write cycle at an
initial time

610

To write a data value represented by a
first resistance range, apply a first
verify operation having a first verify
period, starting after the initial time and
ending after a first time delay

620

To write a data value represented by a
second resistance range, apply a second
verify operation having a second verify period
longer than the first verify period, starting
after the initial time and ending after a third
time delay longer than the second time delay

625

Apply a first write operation having a
first write period, starting after a
second time delay, and ending before
a final time delay

630

Apply a second write operation having a
second write period shorter than the first write
period, starting after a fourth time delay, and
ending before the final time delay

635

End the write cycle at the
final time delay

640

Figure 6

700

710 — Start a write cycle at an initial time

720 — To write a data value represented by a first resistance range, apply a first write operation having a first write period, starting after the initial time and ending after a third time delay

725 — To write a data value represented by a second resistance range, apply a second write operation having a second write period shorter than the first write period, starting after the initial time and ending after a first time delay

730 — Apply a first verify operation having a first verify period shorter than a second verify period, starting after a fourth time delay, and ending before a final time delay

735 — Apply a second verify operation having the second verify period, starting after a second time delay shorter than the third time delay, and ending before the final time delay

740 — End the write cycle at the final time delay

Figure 7

800

890 — Other Circuitry

880 — COLUMN DECODER

885

870 — PAGE BUFFER

885

860 — Memory Array

865

810 — CONTROLLER

Write a data value to a memory cell, the data value represented by first and second programmable resistance ranges, in a write cycle shorter than the sum of a longer write period and a longer verify period

830 — ADDRESS

845

810 — ROW DECODER

810

820 — BIASING ARRANGEMENT SUPPLY VOLTAGES

Figure 8

STAGGERED WRITE AND VERIFY FOR PHASE CHANGE MEMORY

BACKGROUND

1. Field of the Invention

The present application relates to programmable resistance memory, including phase change memory, and more particularly to a write cycle for a memory device.

2. Description of Related Art

In a phase change memory and other programmable resistance memory, to write a data value represented by a resistance range to a memory cell, a sequence of alternating verify operations and write operation can be applied to the memory cell. A phase change memory can be a bit-alternative memory, where a verify operation and a write operation to set a first memory cell to a first resistance range can be in the same write cycle as a second verify operation and a second write operation to set a second memory cell to a second resistance range. To write two data values represented by two different resistance ranges to two memory cells, verify operations on the two memory cells can both start at an initial time, and subsequent write operations on the two memory cells can both start at a secon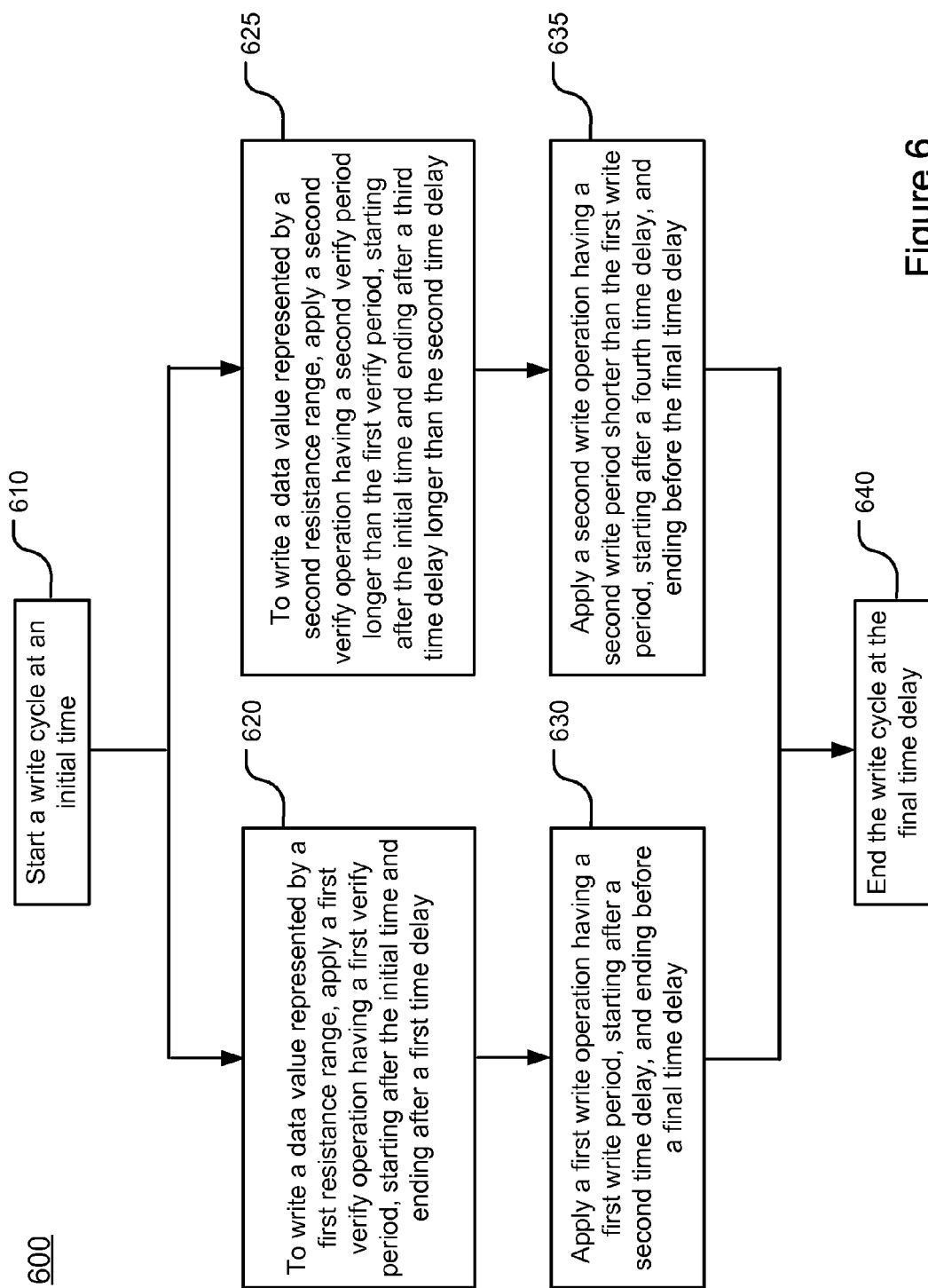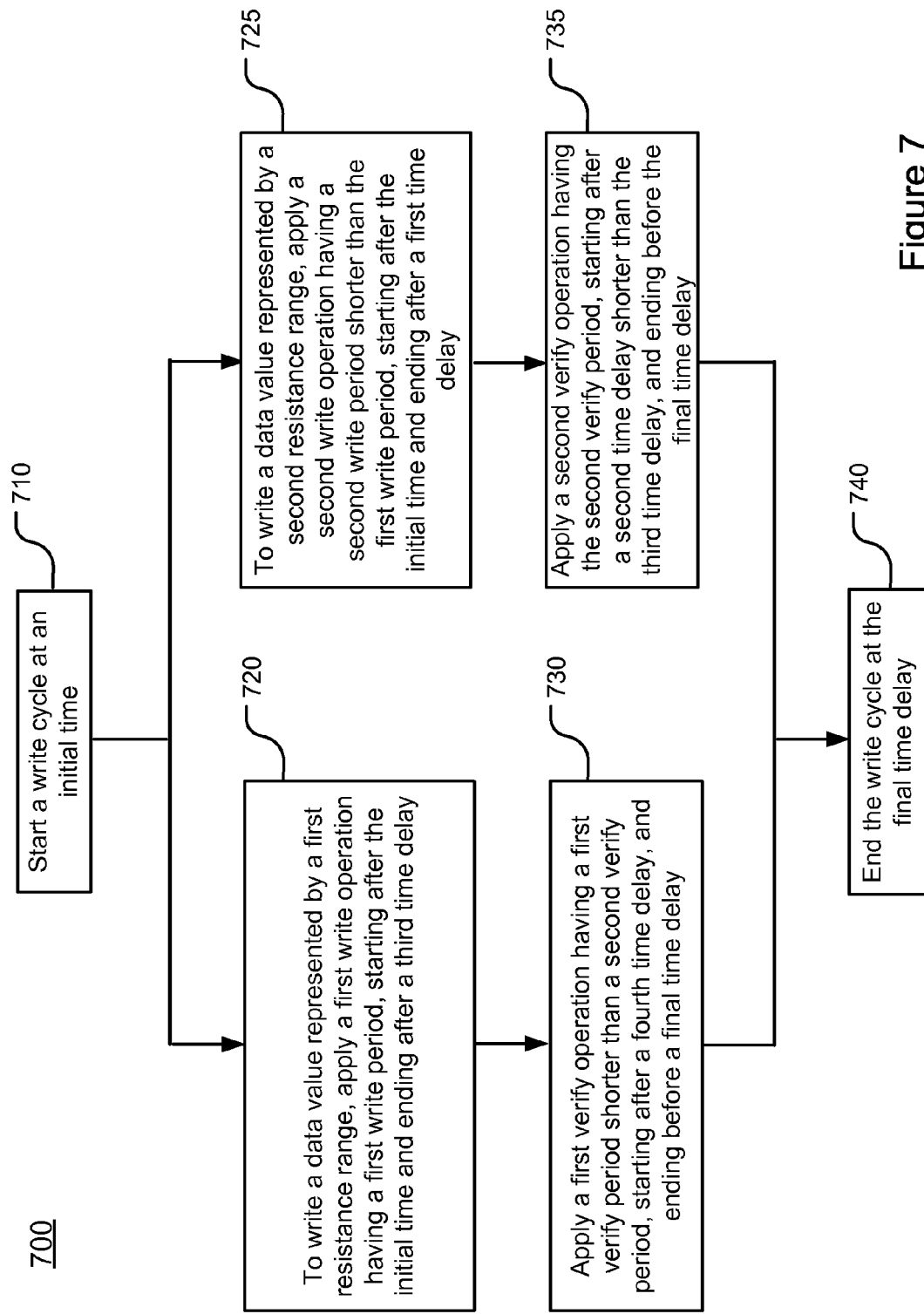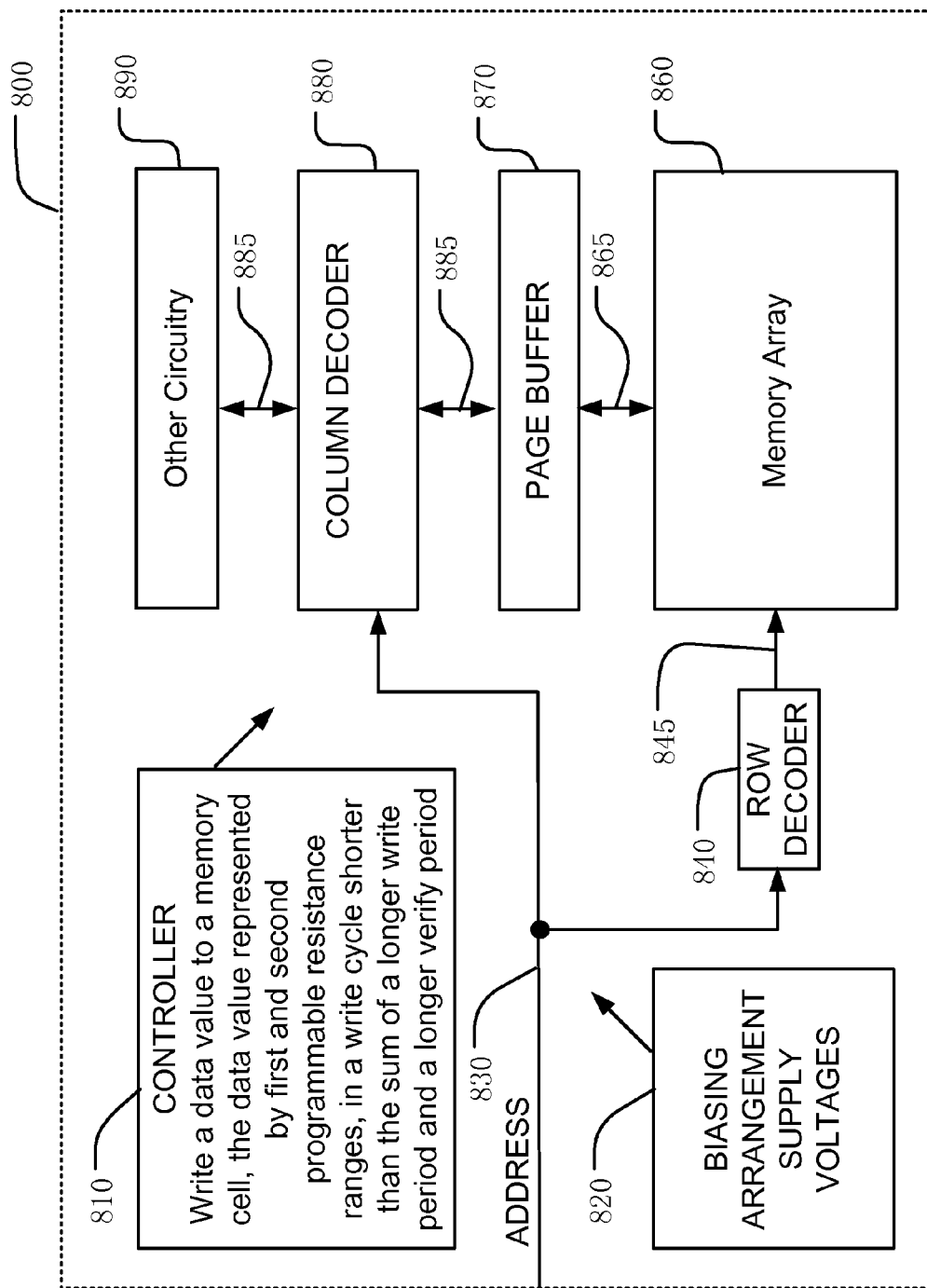d time, in the same write cycle. However, depending on the data value, a verify operation is either longer or shorter than a write operation. Consequently, a longer write operation after a shorter verify operation on a first memory cell waits for a longer verify operation on a second memory cell to end before the longer write operation on the first memory cell can start. Similarly, the longer verify operation after the shorter write operation on the second memory cell waits for the longer write operation on the first memory cell to end before the longer write operation for the second memory cell can start. Such waiting degrades the overall memory performance.

It is desirable to provide a method to improve the overall memory performance when writing data values represented by different resistance ranges in the same write cycles.

SUMMARY

A method for storing a data value in a memory cell is provided. The memory cell can be in a memory, such as a phase change memory where a plurality of memory cells stores data values represented by different programmable resistance ranges. The data value includes one of a first data value and a second data value respectively represented by a first and a second programmable resistance ranges.

One embodiment described herein includes, within a write cycle, storing the first data value in the memory cell by applying a first verify operation having a first verify period and a first write operation having a first write period, or storing the second data value in the memory cell by applying a second verify operation having a second verify period longer than the first verify period and a second write operation having a second write period shorter than the first write period. The write cycle is shorter than a sum of the first write period and the second verify period.

The first verify period starts after an initial time of the write cycle and ends after a first time delay. The first write period starts after a second time delay and ends before a final time delay. The second verify period starts after the initial time and ends after a third time delay longer than the second time delay. The second write period starts after a fourth time delay and ends before the final time delay.

The first verify period and the first write period are dependent on the first programmable resistance range. The second

verify period and the second write period are dependent on the second programmable resistance range.

The plurality of memory cells, including a first memory cell, is coupled to a plurality of bit lines, where the first verify operation and the first write operation can be applied to the first memory cell via a first bit line in the plurality of bit lines and coupled to the memory cell. During the write cycle when the first data value is stored in the first memory cell, the second data value can be stored in a second memory cell in the plurality of memory cells via a second bit line in the plurality of bit lines by applying a second verify operation having the second verify period and a second write operation having the second write period.

Resistance values in the first resistance range can be lower than resistance values in the second resistance range, and the first write operation can have a voltage amplitude lower than a voltage amplitude of the second write operation and higher than a voltage amplitude of the first verify operation and the second verify operation.

In an alternative embodiment described herein, the first write period starts after an initial time of the write cycle and ends after a third time delay. The first verify period starts after a fourth time delay and ends before a final time delay. The second write period starts after the initial time and ends after a first time delay. The second verify period starts after a second time delay shorter than the third time delay and ends before the final time delay.

A memory device is also described configured to execute the methods described herein.

Other aspects and advantages of the present invention can be seen on review of the drawings, the detailed description and the claims, which follow.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a waveform diagram illustrating using waiting time between verify and write operations when writing data values represented by programmable resistance ranges.

FIG. 2 is a waveform diagram illustrating an implementation of a method for writing a data value to a memory cell, where the data value is represented by first and second programmable resistance ranges.

FIG. 3 is a waveform diagram illustrating first and second sequences of operations for writing data values represented by first and second programmable resistance ranges.

FIG. 4 is a waveform diagram illustrating an alternative implementation of a method for writing a data value to a memory cell, where the data value is represented by first and second programmable resistance ranges.

FIG. 5 is a waveform diagram illustrating an alternative implementation of a method for writing a data value to a memory cell, where write operations for writing the data value represented by the first and second programmable resistance ranges can have different voltage amplitudes.

FIG. 6 is a flowchart illustrating an implementation of a method for writing a data value to a memory cell, where the data value is represented by first and second programmable resistance ranges.

FIG. 7 is a flowchart illustrating an alternative implementation of the method for writing a data value to a memory cell, where the data value is represented by first and second programmable resistance ranges.

FIG. 8 is a simplified block diagram of an integrated circuit memory including a controller configured with logic to execute the method described herein.

DETAILED DESCRIPTION

A detailed description of various embodiments is described with reference to the Figures. The following

description will typically be with reference to specific structural embodiments and methods. It is to be understood that there is no intention to limit the invention to the specifically disclosed embodiments and methods but that the invention may be practiced using other features, elements, methods and embodiments. Preferred embodiments are described to illustrate the present invention, not to limit its scope, which is defined by the claims. Those of ordinary skill in the art will recognize a variety of equivalent variations on the description that follows. Like elements in various embodiments are commonly referred to with like reference numerals.

FIG. 1 is a waveform diagram illustrating using waiting time between verify and write operations when writing data values represented by programmable resistance ranges. In FIG. 1, a first sequence of alternating verify operations and write operations for writing a data value represented by a first programmable resistance range (e.g. low resistance) is illustrated by waveforms applied to a first bit line (BL1 voltage). A second sequence of alternating verify operations and write operations for writing a data value represented by a second programmable resistance range (e.g. high resistance) is illustrated by waveforms applied to a second bit line (BL2 voltage). A verify operation verifies whether a memory cell is set to an expected resistance range. If the memory cell is not set to an expected resistance range, a subsequent write operation is applied.

In a bit alternative memory, such as a phase change memory, a memory cell can be written to a data value represented by a low resistance, while another memory cell can be written to another data value represented by a high resistance, in a write cycle. For each of the data values, the write cycle can include a verify operation followed by a write operation. Depending on the data value, a verify operation is either longer or shorter than a write operation.

The verify operation for high resistance can be slower than the verify operation for low resistance because of lower cell current associated with high resistance than with low resistance. For phase change memory, the write operation for high resistance is faster than the write operation for low resistance because of faster quench time associated with high resistance than with low resistance.

As illustrated in FIG. 1, in a first write cycle, to write a data value represented by a low resistance, a shorter verify operation 110 is followed by a longer write operation 130 with a first waiting time 115 in between, while to write a data value represented by a high resistance, a longer verify operation 120 is followed by a shorter write operation 140 with a second waiting time 145 after the shorter write operation 140.

The shorter verify operation 110 and the longer verify operation 120 both start after an initial time T0 of the first write cycle. The shorter verify operation 110 ends at a first time delay T1, before the longer verify operation 120 ends at a second time delay T2. The longer write operation 130 waits through the first waiting time 115 for the longer verify operation 120 to end.

The longer write operation 130 and the shorter write operation 140 then both start after a third time delay T3. The longer write operation 130 ends before a final time delay TX. The shorter write operation 140 ends at a fourth time delay T4, before the longer write operation 130 ends. The next longer verify operation 120 for writing a data value represented by a high resistance waits through the second waiting time 145 in the first write cycle, and starts after the final time delay TX of the first write cycle or the initial time T0 of the second write cycle.

Consequently, the final time delay TX is equal to or greater than the sum of the longer write operation 130 and the longer verify operation 120.

FIG. 2 is a waveform diagram illustrating an implementation of a method for writing a data value to a memory cell, where the data value is represented by first and second programmable resistance ranges. For instance, the first resistance range can have resistance values lower than resistance values in the second resistance range. The data value is written in a write cycle. The write cycle includes a first sequence of alternating verify operations and write operations for writing a first data value represented by the first programmable resistance range, and a second sequence of alternating verify operations and write operations for writing a second data value represented by the second programmable resistance range. A verify operation is applied after a write operation. If the verify operation determines that the memory cell is not set to an expected resistance range by the previous write operation, another write operation is then applied. First and second verify operations, and first and second write operations as referred to in FIG. 2 are examples for operations in the first and second sequences of operations.

As illustrated in the example of FIG. 2, the write cycle starts at an initial time (e.g. T0) and ends at a final time delay (e.g. TX). To write a first data value represented by the first resistance range (e.g. Low Resistance or Low R), a first verify operation (e.g. 210) is applied to the memory cell. The first verify operation has a first verify period. The first verify period starts after the initial time (e.g. T0) and ends after a first time delay (e.g. T1). A first write operation (e.g. 230) is subsequently applied to the memory cell. The first write operation has a first write period. The first write period starts after a second time delay (e.g. T2) and ends before the final time delay (e.g. TX).

To write a second data value represented by the second resistance range (e.g. High Resistance or High R) in parallel to a second memory cell, a second verify operation is applied to the second memory cell (e.g. 220). The second verify operation has a second verify period longer than the first verify period. The second verify period starts after the initial time (e.g. T0) and ends after a third time delay (e.g. T3) longer than the second time delay (e.g. T2). A second write operation is subsequently applied to the second memory cell (e.g. 240). The second write operation has a second write period shorter than the first write period. The second write period starts after a fourth time delay (e.g. T4) and ends before the final time delay (e.g. TX). Consequently, the method as illustrated in the example of FIG. 2 does not use the first and second waiting times (e.g. 115, 145) as in the method as illustrated in FIG. 1.

In this implementation of the method, the final time delay is shorter than the sum of the first write period and the second verify period. In comparison, the write cycle described in connection with FIG. 1 is equal to or greater than the sum of the longer write operation and the longer verify operation. Consequently, the method described in connection with FIG. 2 can shorten the write cycle, and improve operating speed of the memory device.

As illustrated in the example of FIG. 2, the first and second write operations for writing the data value represented by the first and second programmable resistance ranges can have a same voltage amplitude. In an alternative implementation, the first write operation for programming low resistance (e.g. 230) can have a voltage amplitude lower than a voltage amplitude of the second write operation for programming high resistance (e.g. 240) and higher than a voltage amplitude of the first verify operation and the second verify operation (e.g. 210, 220).

The plurality of memory cells in the memory are coupled to a plurality of bit lines. Within a write cycle, the first verify operation and the first write operation can be applied to a first memory cell via a first bit line in the plurality of bit lines and coupled to the first memory cell, while the second verify operation and the second write operation can be applied in parallel to a second memory cell via a second bit line in the plurality of bit lines and coupled to the second memory cell.

FIG. 3 is a waveform diagram illustrating a first sequence of alternating verify operations and write operations for writing a first data value represented by the first programmable resistance range, and a second sequence of alternating verify operations and write operations for writing a second data value represented by the second programmable resistance range. Waveforms for voltage applied to a first bit line (BL1 voltage) correspond to the first sequence. Waveforms for voltage applied to a second bit line (BL2 voltage) correspond to the second sequence. Verify operations and write operations in the first and second sequences are as described in connection with FIG. 2. The first and second write cycles are examples for more write cycles in the first and second sequences.

A verify operation verifies whether a memory cell is set to an expected resistance range. If the memory cell is not set to an expected resistance range, a subsequent write operation is applied, until the memory cell is in the expected resistance range or until a pre-determined number of verify/write operations has been executed. When memory cells in a byte (e.g. 8 bits), a word (e.g. 16 bits), a page (e.g. multiple words), or up to a full memory device have either been set to the expected resistance ranges or have reached the pre-determined number of verify/write operations, a final verify is executed to verify the memory cells that are expected to be set to the first resistance range (e.g. 370, low resistance) or the second resistance range (e.g. 380, high resistance). Results from the final verify can be used for specification about data retention of the memory device.

FIG. 4 is a waveform diagram illustrating an alternative implementation of a method for writing a data value to a memory cell, where the data value is represented by first and second programmable resistance ranges. The alternative implementation can be used in an application where a write operation can be executed before a verify operation. For instance, a first write operation to write a first data value represented by the first resistance range to a first memory cell, and/or a second write operation to write a second data value represented by the second resistance range to a second memory cell, can be applied after an initial time in a write cycle, before any verify operations are applied in the write cycle.

As illustrated in the example of FIG. 4, the write cycle starts at an initial time (e.g. T0) and ends at a final time delay (e.g. TX). To write a first data value represented by the first resistance range (e.g. Low Resistance or Low R) to the memory cell, a first write operation is applied to the first memory cell (e.g. 430). The first write operation has a first write period. The first write period starts after the initial time (e.g. T0) and ends after a third time delay (e.g. T3). A first verify operation (e.g. 410) is subsequently applied to the memory cell. The first verify operation has a first verify period. The first verify period starts after a fourth time delay (e.g. T4) and ends before the final time delay (e.g. TX). Between the first write operation and the first verify operation, there can be a minimum setup time required for the first verify operation.

To write a second data value represented by the second resistance range (e.g. High Resistance or High R) in parallel

to a second memory cell, a second write operation (e.g. 440) is applied to the second memory cell. The second write operation has a second write period shorter than the first write period. The second write period starts after the initial time (e.g. T0) and ends after a first time delay (e.g. T1). A second verify operation (e.g. 420) is subsequently applied to the memory cell. The second verify operation has a second verify period longer than the first verify period. The second verify period starts after a second time delay (e.g. T2) shorter than the third time delay and ends before the final time delay (e.g. TX). Between the second write operation and the second verify operation, there can be a minimum setup time required for the second verify operation.

In this implementation, the first and second write operations for writing the data value represented by the first and second programmable resistance ranges can have a same voltage amplitude. The final time delay is shorter than the sum of the first write period and the second verify period. Consequently, the method described in connection with FIG. 4 can shorten the write cycle, and improve operating speed of the memory device, in comparison to the method described in connection with FIG. 1.

FIG. 5 is a waveform diagram illustrating an alternative implementation of a method for writing a data value to a memory cell, where write operations for writing the data value represented by the first and second programmable resistance ranges can have different voltage amplitudes. Like elements in FIG. 5 are referred to with like reference numerals in FIG. 4.

In the example shown in FIG. 5, to write a first data value represented by the first resistance range (e.g. Low Resistance or Low R), a first write operation (e.g. 530) is applied to the memory cell. The first write operation has a first write period longer than the second write period of the second write operation (e.g. 440). The first write period starts after the initial time (e.g. T0) and ends after a third time delay (e.g. T3) longer than the second time delay (e.g. T2). A first verify operation (e.g. 410) is subsequently applied to the memory cell. The first verify operation has a first verify period shorter than the second verify period of the second verify operation (e.g. 420). The first verify period starts after a fourth time delay (e.g. T4) and ends before the final time delay (e.g. TX). Between the first write operation and the first verify operation, there can be a minimum setup time required for the first verify operation.

As illustrated in the example of FIG. 5, the first write operation for programming low resistance (e.g. 530) has a voltage amplitude V2 lower than a voltage amplitude V3 of the second write operation for programming high resistance (e.g. 440) and higher than a voltage amplitude V1 of the first verify operation and the second verify operation (e.g. 420, 410). For instance, voltage amplitudes V1, V2 and V3 can be 0.4V, 2V and 2.5V, respectively. In comparison, the voltage amplitude for programming low resistance and the voltage amplitude for programming high resistance in the embodiments illustrated by FIGS. 2-4 can be the same, for example, at 2.5V. The voltage amplitude of the verify operations in the embodiments illustrated by FIGS. 2-4 can be at 0.4V.

FIG. 6 is a flowchart illustrating an implementation of a method for writing a data value to a memory cell, where the data value is represented by first and second programmable resistance ranges. For instance, the first resistance range can have resistance values lower than resistance values in the second resistance range. The data value is written in a write cycle. The write cycle starts at an initial time (Step 610), and ends at a final time delay (Step 640).

To write a first data value represented by the first resistance range, a first verify operation is applied to the memory cell

(Step **620**). The first verify operation has a first verify period, and the first verify period starts after an initial time of a write cycle and ends after a first time delay. A first write operation is subsequently applied to the memory cell (Step **630**). The first write operation has a first write period, and the first write period starts after a second time delay and ends before a final time delay.

To write a second data value represented by the second resistance range, a second verify operation is applied (Step **625**). The second verify operation has a second verify period longer than the first verify period. The second verify period starts after the initial time and ends after a third time delay longer than the second time delay. A second write operation is subsequently applied to the memory cell (Step **635**). The second write operation has a second write period shorter than the first write period. The second write period starts after a fourth time delay and ends before the final time delay.

In this implementation of the method, the final time delay is shorter than the sum of the first write period and the second verify period.

A first data value represented by the first resistance range can be written to a first memory cell, while a second data value represented by the second resistance range can be written in parallel to a second memory cell, in a same write cycle. The initial time and the final time delay of the write cycle are the same for writing data values represented by the first and second resistance ranges to the first memory cell and the second memory cell, respectively.

FIG. **7** is a flowchart illustrating an alternative implementation of the method for writing a data value to a memory cell, where the data value is represented by first and second programmable resistance ranges. The data value is written in a write cycle. The write cycle starts at an initial time (Step **710**), and ends at a final time delay (Step **740**).

To write a first data value represented by the first resistance range, a first write operation is applied (Step **720**). The first write operation has a first write period longer than the second write period of the second write operation (e.g. **440**, FIG. **4**). The first write period starts after the initial time and ends after a third time delay longer than a second time delay. A first verify operation is subsequently applied (Step **730**). The first verify operation has a first verify period shorter than the second verify period of the second verify operation (e.g. **420**, FIG. **4**). The first verify period starts after a fourth time delay and ends before the final time delay.

To write a second data value represented by the second resistance range, a second write operation is applied. The second write operation has a second write period, and the second write period starts after the initial time of the write cycle and ends after a first time delay (Step **725**) shorter than the second time delay. A second verify operation is subsequently applied (Step **735**). The second verify operation has a second verify period. The second verify period starts after the second time delay and ends before a final time delay.

In the alternative implementation of the method, the final time delay is shorter than the sum of the first write period and the second verify period.

FIG. **8** is a simplified block diagram of an integrated circuit memory including a controller **810** configured to implement a method for operating the integrated circuit memory **800**. The controller **810** is coupled to the memory array **860**. The method can include writing a data value to a memory cell, where the data value is represented by first and second programmable resistance ranges. To write a first data value represented by the first resistance range, a first verify operation and subsequently a first write operation are applied to the memory cell. The first verify operation has a first verify

period, and the first verify period starts after an initial time of a write cycle and ends after a first time delay. The first write operation has a first write period, and the first write period starts after a second time delay and ends before a final time delay.

To write a second data value represented by the second resistance range, a second verify operation and subsequently a second write operation are applied. The second verify operation has a second verify period longer than the first verify period. The second verify period starts after the initial time and ends after a third time delay longer than the second time delay. The second write operation has a second write period shorter than the first write period, and the second write period starts after a fourth time delay and ends before the final time delay. The final time delay is shorter than the sum of the first write period and the second verify period.

In an alternative embodiment described herein, the method can include writing a first data value represented by the first resistance range by applying a first write operation having a first write period, and subsequently a first verify operation having a first verify period, and writing a second data value represented by the second resistance range by applying a second write operation having a second write period longer than the first write period, and subsequently a second verify operation having a second verify period shorter than the first verify period, such that the final time delay is shorter than the sum of the first verify period and the second write period.

The controller **810**, implemented for example as a state machine, provides signals to control the application of bias arrangement supply voltages generated or provided through the voltage supply or supplies in block **820** to carry out the various operations described herein. These operations include read, write, and refresh operations. The controller can be implemented using special-purpose logic circuitry as known in the art. In alternative embodiments, the controller comprises a general-purpose processor, which can be implemented on the same integrated circuit, which executes a computer program to control the operations of the device. In yet other embodiments, a combination of special-purpose logic circuitry and a general-purpose processor can be utilized for implementation of the controller.

In some embodiments, the memory array **860** can include single levels of cells (SLC). In other embodiments, the memory array **860** can include multiple levels of cells (MLC). A row decoder **840** is coupled to a plurality of word lines **845** arranged along rows in the memory array **860**. Column decoders in block **880** are coupled to a set of page buffers **870**, in this example via data bus **875**. Global bit lines **865** are coupled to local bit lines (not shown) arranged along columns in the memory array **860**. Addresses are supplied on bus **830** to column decoders in block **880** and row decoder in block **840**. Data is supplied via the line **885** from other circuitry **890** (including for example input/output ports) on the integrated circuit, such as a general purpose processor or special purpose application circuitry, or a combination of modules providing system-on-a-chip functionality supported by the memory array **860**.

While the present invention is disclosed by reference to the preferred embodiments and examples detailed above, it is to be understood that these examples are intended in an illustrative rather than in a limiting sense. It is contemplated that modifications and combinations will readily occur to those skilled in the art, which modifications and combinations will be within the spirit of the invention and the scope of the following claims.

What is claimed is:

1. A method for storing a data value in a memory cell, the data value including one of a first data value and a second data value respectively represented by a first and a second programmable resistance ranges, comprising:

within a write cycle, storing the first data value in the memory cell by applying a first verify operation having a first verify period and a first write operation having a first write period, or storing the second data value in the memory cell by applying a second verify operation having a second verify period longer than the first verify period and a second write operation having a second write period shorter than the first write period,

wherein the write cycle is shorter than a sum of the first write period and the second verify period.

2. The method of claim 1, wherein the first verify period starts after an initial time of the write cycle and ends after a first time delay, the first write period starts after a second time delay and ends before a final time delay, the second verify period starts after the initial time and ends after a third time delay longer than the second time delay, and the second write period starts after a fourth time delay and ends before the final time delay.

3. The method of claim 1, wherein the first verify period and the first write period are dependent on the first programmable resistance range, and the second verify period and the second write period are dependent on the second programmable resistance range.

4. The method of claim 1, the memory comprising:

a plurality of memory cells, including said memory cell, coupled to a plurality of bit lines, wherein the first verify operation and the first write operation are applied to the memory cell via a first bit line in the plurality of bit lines and coupled to the memory cell.

5. The method of claim 4, including wherein during said write cycle, the first data value is stored in said memory cell, and during said write cycle, storing the second data value in a second memory cell in said plurality of memory cells via a second bit line in the plurality of bit lines by applying a second verify operation having said second verify period and a second write operation having said second write period.

6. The method of claim 1, wherein resistance values in the first resistance range are lower than resistance values in the second resistance range, and the first write operation has a voltage amplitude lower than a voltage amplitude of the second write operation and higher than a voltage amplitude of the first verify operation and the second verify operation.

7. The method of claim 1, wherein the first write period starts after an initial time of the write cycle and ends after a third time delay, the first verify period starts after a fourth time delay and ends before a final time delay, the second write period starts after the initial time and ends after a first time delay, and the second verify period starts after a second time delay shorter than the third time delay and ends before the final time delay.

8. A memory, comprising:

a plurality of memory cells storing data values being represented by first and second programmable resistance ranges; and

a controller coupled to the memory cells, including logic to write a data value to a memory cell in the plurality of memory cells, the logic includes:

to write a first data value represented by the first resistance range, logic to apply a first verify operation having a first verify period; and logic to apply a first write operation having a first write period; and

to write a second data value represented by the second resistance range, logic to apply a second verify operation having a second verify period longer than the first verify period; and logic to apply a second write operation having a second write period shorter than the first write period,

wherein a write cycle for writing one of the first and second data values is shorter than a sum of the first write period and the second verify period.

9. The memory of claim 8, wherein the first verify period starts after an initial time of the write cycle and ends after a first time delay, the first write period starts after a second time delay and ends before a final time delay, the second verify period starts after the initial time and ends after a third time delay longer than the second time delay, and the second write period starts after a fourth time delay and ends before the final time delay.

10. The memory of claim 8, wherein the first verify period and the first write period are dependent on the first programmable resistance range, and the second verify period and the second write period are dependent on the second programmable resistance range.

11. The memory of claim 8, the memory comprising:

a plurality of memory cells coupled to a plurality of bit lines, wherein the first verify operation and the first write operation are applied to the memory cell via a first bit line in the plurality of bit lines and coupled to the memory cell,

wherein the second verify operation and the second write operation are applied in parallel to a second memory cell via a second bit line in the plurality of bit lines and coupled to the second memory cell.

12. The memory of claim 8, wherein resistance values in the first resistance range are lower than resistance values in the second resistance range, and the first write operation has a voltage amplitude lower than a voltage amplitude of the second write operation and higher than a voltage amplitude of the first verify operation and the second verify operation.

13. A memory, comprising:

a plurality of memory cells storing data values being represented by first and second programmable resistance ranges; and

a controller coupled to the memory cells, including logic to write a data value to a memory cell in the plurality of memory cells, the logic includes:

to write a first data value represented by the first resistance range, logic to apply a first write operation having a first write period; and logic to apply a first verify operation having a first verify period; and

to write a second data value represented by the second resistance range, logic to apply a second write operation having a second write period shorter than the first write period; and logic to apply a second verify operation having a second verify period longer than the first verify period,

wherein a write cycle for writing one of the first and second data values is shorter than a sum of the first write period and the second verify period.

14. The memory of claim 13, wherein the first write period starts after an initial time of the write cycle and ends after a third time delay, the first verify period starts after a fourth time delay and ends before a final time delay, the second write period starts after the initial time and ends after a first time delay, and the second verify period starts after a second time delay shorter than the fourth time delay and ends before the final time delay.

15. The memory of claim **13**, the memory comprising:

a plurality of memory cells coupled to a plurality of bit lines, wherein the first verify operation and the first write operation are applied to the memory cell via a first bit line in the plurality of bit lines and coupled to the memory cell,

wherein the second verify operation and the second write operation are applied in parallel to a second memory cell via a second bit line in the plurality of bit lines and coupled to the second memory cell.

16. The memory of claim **13**, wherein resistance values in the first resistance range are lower than resistance values in the second resistance range, and the first write operation has a voltage amplitude lower than a voltage amplitude of the second write operation and higher than a voltage amplitude of the first verify operation and the second verify operation.

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